REMARKS/ARGUMENTS

Claims 21, 24, 27, 28, 31, and 36 - 38 are pending.

Claims 21 and 36 were rejected under 35 U.S.C. § 102(b) based on Berezin, U.S. Patent No. 5,777,901.

Claim 27 was rejected under 35 U.S.C. § 103(a) for allegedly being obvious in view of Berezin and Atchison, U.S. Patent No. 6,324,481.

Claims 24, 28, 31, and 37 - 38 were rejected under 35 U.S.C. § 103(a) f or allegedly being obvious in view of Berezin and Hashimoto, U.S. Patent No. 6,334,209.

Claims 21 and 36 have been amended to further clarify the claimed invention, and therefore distinguish the cited art. The claims have also been amended to correct a minor informality. In particular, the term "and" was replace with "or" for consistent usage of the phrase "said particles or said pattern defects." Claim 36 has been amended to correct a similar informality.

The present invention is directed to defect detection in a wafer inspection station. As noted in a response to an earlier Office action, an aspect of the invention is the computation of probability metrics for defects which are located in specific regions (logic blocks) which comprise the logic circuitry of a semiconductor chip formed on a wafer. As an example, an illustrative embodiment of this aspect of the invention is described in on page 14.

Independent claim 21, as originally presented, recites a storage device of an analysis unit to store "position information of regions of a circuit pattern to be formed on said object" to be inspected. There is a "calculation device for identifying particles or pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities ... based on location of said particles or said pattern defects in said regions." (emphasis added).

Likewise, independent claim 36 recites "identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns" and "calculating failure probabilities based on sizes of said particles or said pattern defects in said region and on their location in said region." (emphasis added).

As with the references cited in an earlier Office action, the references cited in the instant Office action do not teach or render obvious this aspect of the claimed invention.

Claim 21: "storage device"

Applicant's recited "storage device" in claim 21 was alleged to be shown in col. 6, lines 33 - 55 of Berezin et al. As mentioned above, the recited storage device stores "position information of regions of a circuit pattern to be formed on said object" to be inspected. Comparing to Berezin et al., they describe defect data contained in records stored in a database of a scan tool. *Col. 6, lines 37 - 38.* Each record stores information concerning the defects, including their X-, Y-locations on the wafer *(line 49)*, defect size information *(line 50)*, and classification code identifying a type of defect *(lines 52 - 65)*.

The defect data of Berezin et al. do not include "position information of regions of a circuit pattern to be formed on said object" to be inspected. Moreover, a review of Berezin et al. does not reveal that their defect data contemplates the inclusion of data relating to position information for "regions of a circuit pattern." For at least this reason, the Section 102 rejection of the claim 21 is believed to be overcome.

Claim 21: "calculation device"

Applicant's recited "calculation device" in claim 21 was alleged to be shown in col. 3, lines 23 - 45 of Berezin et al. The recited calculation device identifies "particles or pattern defects that are correspondingly positioned in said regions, and [calculates] failure probabilities ... based on location of said particles or said pattern defects in said regions." Berezin et al. disclose collecting defect data (type and size) for each layer of a substrate. The defect data is stacked according to the layers to identify the onset of a defect and number of occurrences. A kill factor is assigned according to a set of rules, from which failure probabilities are determined. *Col. 3, lines 28 - 42.*

Berezin et al. do not disclose identifying "particles or pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities ... based on location of said particles or said pattern defects in said regions." Though Berezin et al. collect defect data for each layer of a substrate, such data is not identified with defects that are

correspondingly positioned in said regions [of a circuit pattern]. The rules used by Berezin et al. to assign a kill factor do not include location of said particles or said pattern defects in said regions [of a circuit pattern].

For at least this reason, the Section 102 rejection of claim 21 is believed to be overcome.

Claim 36: "identifying positions"

Claim 36 recites "identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns."

Berezin et al. were cited at col. 1, lines 40 - 55, col. 2, lines 64 -67, and col. 3, generally at lines 1 - 26 for allegedly teaching this aspect of the claimed invention. Berezin et al. describe recording defects according to their coordinates, size, or other parameters. *Col. 1, lines 46 - 47.* Recording the coordinates of defects on a wafer simply identifies the defect one the wafer, and does not constitute location in a region of said circuit patterns. Thus, Berezin et al. do not teach or even suggest correlating or otherwise associating location on a wafer with circuit patterns. Moreover, the mention of "or other parameters" does not in and of itself suggest locations on a circuit pattern, absent an improper incorporation of teachings from the present invention.

Consequently, the Section 102 rejection of claim 36 is believed to be overcome, for this reason alone.

Claim 36: "calculating failure probabilities"

Claim 36 further recites "calculating failure probabilities based on sizes of said particles or said pattern defects in said region and on their location in said region."

Berezin et al. was cited at col. 3, lines 23 - 45 for teaching that failure probabilities are calculated based on at least size. Claim 36 has been amended to more clearly recite an aspect of the invention that is believed to be distinguishable over the cited art, namely, that probabilities are "based on sizes of said particles or said pattern defects in said region [of said circuit pattern] and on their location in said region." As discussed above, Berezin et al. do

not teach this aspect of the invention. Therefore, the Section 102 rejection of claim 36 is believed to be overcome for at least this reason.

Dependent Claims

Claims depending from independent claims 21 and 36 are believed to be allowable based on the allowability of their respective independent claims. The additional art cited in the Section 103 rejections of the dependent claims do not teach the foregoing discussed aspects of the present invention as claimed.

As discussed in a response to an earlier Office action, Atchison '481 does not disclose the foregoing discussed aspects of the present invention.

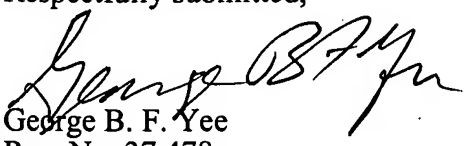
Hashimoto et al. disclose a technique for inspecting an exposure mask. As described in col. 3, lines 49 - 67, inspection of an exposure mask involves inputting the CAD layout of the mask pattern to a simulator which simulates the actual lithographic process. *Col. 3, lines 59 - 63.* Hashimoto et al. was cited for disclosing a system LSI with logic and memory portions and mask layout data. *O.A. at page 5, paragraph 9.* However, simulating the lithographic process of an exposure mask does not suggest processing of wafer defects that is based on regions of circuit patterns, as recited in the independent claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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